Process Window Optimizer for pattern based defect prediction on 28nm Metal Layer

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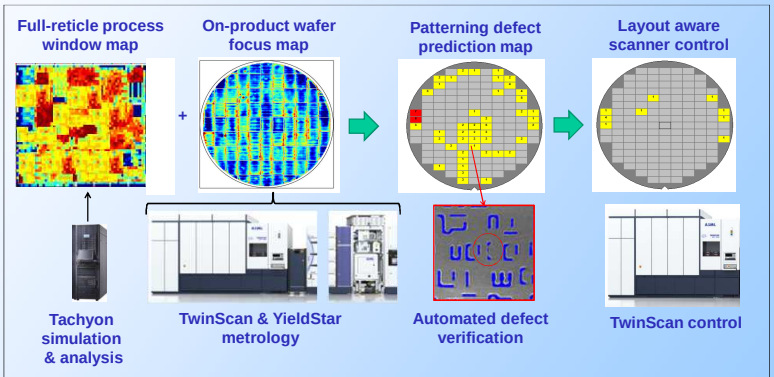
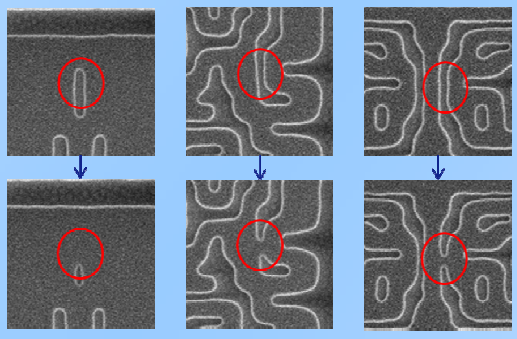
Introduction

Traditional computational lithography applications are not directed towards predicting on-wafer performance. Process of record solutions (e-beam and SEM) to find patterning defect locations are not sensitive enough or have low throughput and need improvements in order to be used as systematic defect detection tools. Process Window Optimizer extends the holistic lithography framework towards prediction, detection and verification of on-product patterning defects. The location of these process window limiting "hotspots" are determined using lithography simulations combined with on-product focus measurements and in-line scanner metrology.



Holistic lithography concept for patterning defect prediction and layout aware scanner control

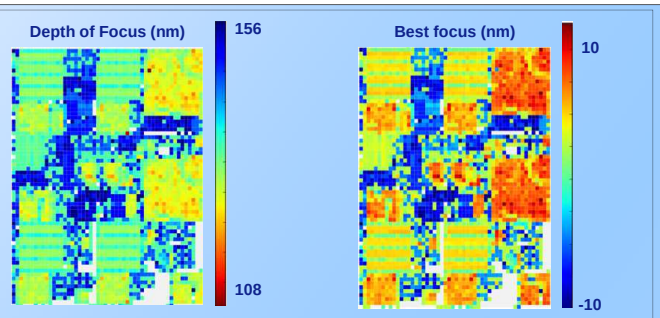


Example of focus induced defects

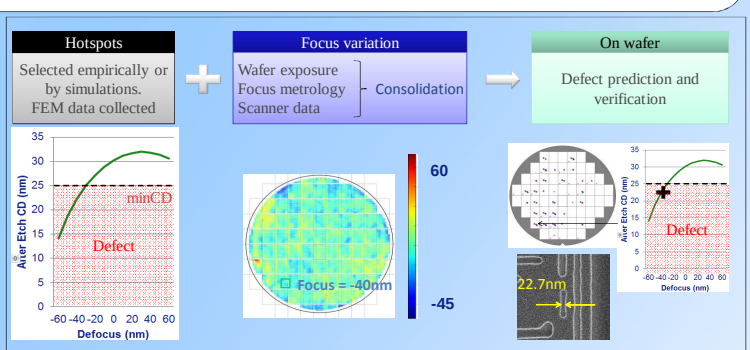
Computational full chip defect prediction flow

The first step in the computational defect prediction flow is to find the patterns across the full chip that will limit the process window the most. Next, CD through focus for each hotspot is simulated. From which we generate a ranked hotspot list together with two maps that characterize the product reticle in terms of best focus and depth of focus. The depth of focus of this product is most critical at the top right and center right of the field. These locations also have a higher best focus offset than the rest of the field. Optimizing scanner focus and levelling control to have a positive defocus at these locations would be a way to reduce defectivity.

The next step in the flow is to combine the simulated CD through focus information with the effective focus values at hotspots locations in the hybrid dense focus map (HDFM). Wherever the defect CD for the corresponding wafer location focus fall below a given threshold, the hotspot will be flagged as a predicted defect.



Full chip simulated depth of focus and best focus per location (white indicates a non-critical region)

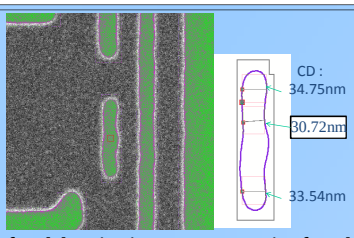


Simplified defect prediction flow

User provided hotspot flow

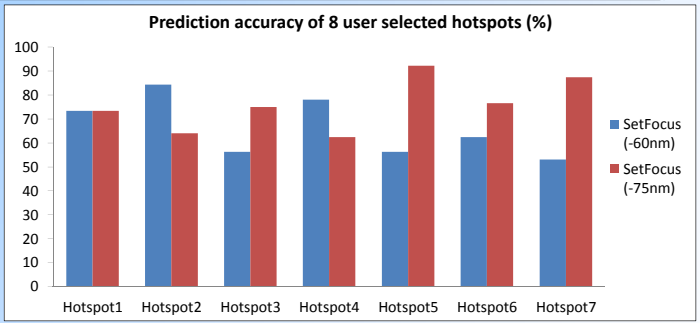
The user provided hotspot flow starts with the user selecting some known hotspots. These can be sourced from simulation and/or from measurement or empirical methods. For each of the studied hotspots, we measured FEM data using CD-SEM image collection, combined with Hitachi contour extraction and applied ASML CD verification tool to collect data through FEM. The focus offsets from the hybrid dense focus map at each position in the wafer are converted to predicted CD values, per hotspot, using the FEM curve. A hotspot is considered a defect if it falls below the CD defect threshold.

In order to generate a significant sample of defects for evaluation purposes this study used an off-focus wafers. A check was done to verify if at the predicted defect locations the SEM revealed a defect or whether no defect was present. On average the -75nm set focus wafer had a higher prediction accuracy since this wafer is exposed more out of focus. This is also dependent of the best focus of each hotspot



Example of neck location in contour extraction for selected hotspot

$$Prediction\ accuracy = \frac{\#\ of\ accurate\ predictions\ (defect\ or\ non-defect)}{Total\ number\ of\ hotspots}$$



Summary

This evaluation has demonstrated the capability of using Process Window Optimizer (PWO) from full chip layout to on-product defect prediction. A computational full chip simulation was combined with on product focus measurements and inline scanner metrology data to predict defect locations. Additionally, user selected hotspots were combined with the hybrid dense focus map and the prediction efficiency of PWO was investigated.

Lithography simulations associated with inline data like dose and focus map is a powerful way to predict patterning issues. PWO demonstrates this and opens a new area for patterning control. PWO will help us to improve our inline defect detection. It will accurately predict defect locations. These locations will be used in our defect detection tool to improve the signal to noise ratio. It will also enable a new way to adjust process within wafer and within field for a given layout. PWO can predict the defect count for several process adjustments and thus help us to find the best within wafer/within field process condition dose/focus to minimize patterning defects.